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## Patent Claims.

1. A component with a logic circuit arrangement with configurable functionality, comprising a plurality of data lines (7), at least a portion of the data lines (7) being assigned at least one element (1) that can be switched between two states with different discrete resistances, by means of which element (1) the data line (7) is enabled or inhibited depending on the switched state, it being possible for the switching state of the element (1) to be stored in nonvolatile fashion and to be changed over rapidly, characterized in that a pass transistor (8) connected into the data line (7) is inhibited or enabled by means of the element (1), or in that the element (1) itself is used as the pass transistor that enables or inhibits the data line (7).
2. The component as claimed in claim 1, characterized in that the element (1) is an element exhibiting a magnetoresistive effect.
3. The component as claimed in claim 2, characterized in that the element (1) is a TMR cell (2).
4. The component as claimed in claim 1, characterized in that the element (1) exhibits a resistance change as a result of a phase change generated during switching, in particular from an amorphous state to a crystalline state.
5. The component as claimed in claim 4, characterized in that the element (1) is an OUM cell.
6. The component as claimed in one of the preceding claims, a pass transistor (8) connected into the data line (7) being inhibited or enabled by means of the element (1), characterized in that only one element (1) or two elements (1)

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coupled to one another and operated in parallel is/are provided for actuating the pass transistor (8).

7. The component as claimed in claim 6, characterized in that two TMR cells (2) are provided, which are driven in inverted fashion.

8. The component as claimed in claim 7, characterized in that the two elements (1), in particular the two TMR cells (2), have a resistance ratio between the two state-related resistances not equal to 1:1, in particular of 1:2 or more.

9. The component as claimed in one of claims 1 to 5, the element (1) itself being used as a pass transistor that enables or inhibits the data line (7), characterized in that the element (1) is connected directly into the data line and directly opens or inhibits the latter, or in that the element is connected in parallel with the data line and short-circuits the latter or behaves in transparent fashion.

10. The component as claimed in claim 9, characterized in that the element (1), in particular the TMR cell (2) or the OUM cell, has/have a resistance ratio between the two state-related resistances of at least 1:5, in particular of at least 1:10 or greater.

11. The component as claimed in one of the preceding claims, characterized in that the switching time for changing over the resistance of the element is  $\leq 5\text{ns}$ , in particular  $\leq 3\text{ns}$